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**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

In re patent application of:

Lily P. LOOI, et al.

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| Serial No.: | 09/752,874 | Group Art Unit: | 2112 |
| Filed: | December 29, 2000 | Examiner: | N. Patel |
| FOR: | APPARATUS AND METHOD FOR INTERRUPT DELIVERY | | |

**PRE-APPEAL BRIEF REQUEST FOR REVIEW**

Mail Stop After Final
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In accordance with the procedures outlined in the Official Gazette published July 12, 2005, applicants respectfully request review of the following clear errors in the final office mailed May 17, 2006, in connection with the above-identified application. A petition for a one month extension time is concurrently filed herewith.

Claims 1-3, 9-12, 16-21, and 25-26 are rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,987,538 (Tavallaei). Claims 1-3, 9-12, 14-21, and 23-26 are rejected under 53 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,944,809 (Olarig). The Examiner commits the following clear errors in making these rejections.

See applicants' response to the final office action, mailed August 18, 2006, for the substantive technical and legal errors in reading these references on the claims. In particular, applicants emphasize that the Examiner commits clear legal error in his claim construction. As is set forth in MPEP § 2111.01(II), "[T]he ordinary and customary meaning of a claim term is the meaning that the term would have to a person of ordinary skill in the art in question at the time of the invention, *i.e.*, as of the effective filing date of the patent application." Several examples set forth in MPEP § 2111.01(II) specifically state that where no definition is provided in the specification, the claim terms should be

interpreted with the ordinary and customary meaning the terms would have to one skilled in the art. The Examiner has not even attempted to identify or set forth what the terms 'scaleable node controller' or 'scalability port switch' would mean to a person of ordinary skill in the art at the time of the invention. This is clear legal error.

The Examiner uses the fact that the specification does not provide a definition for these terms as an excuse to substitute his own, unreasonably broad definition of the terms. In the Examiner's view, any component that performs any control function in connection with any processing element reads on a scaleable node controller. In the Examiner's view any component that performs an I/O function reads on a scalability port switch. Applicants submit that this may be the broadest possible interpretation, but it is not a reasonable interpretation and is also legally erroneous by failing to consider what the disputed terms would mean to one skilled in the art.

The Review Panel can resolve this error by answering a few simple questions. Namely, would one of ordinary skill in the art as of December 29, 2000 (the filing date of the present application), without any knowledge of applicants' own invention, have considered the APIC 14 described by Tavallaei to be a scaleable node controller? Would one of ordinary skill in the art as of December 29, 2000, without any knowledge of applicants' own invention, have considered the I/O APIC 26 described by Tavallaei to be a scalability port switch? Would one of ordinary skill in the art as of December 29, 2000, without any knowledge of applicants' own invention, have considered the cache 107 and LOPIC 306 described by Olarig to be a scaleable node controller? Would one of ordinary skill in the art as of December 29, 2000, without any knowledge of applicants' own invention, have considered the COPIC 312 described by Olarig to be a scalability port switch? Applicants' submit that the answers to all of these questions is no, and the rejection should be withdrawn.

The Examiner relies on a theory of inherency in order to read both the Tavallaei and Olarig on the claim recitations relating to an address for the scaleable node controller. However, the Examiner performs a clearly erroneous factual and legal analysis which fails to meet the burdens required by MPEP § 2112 for a rejection relying on inherency. The Examiner states "[o]ne of ordinary skill in the art would recognize that destination ID is a term that can be used for address." This is the incorrect legal test. Whether or not it 'can be

used' is irrelevant to a legally correct theory of inherency. In order to be inherent, the Examiner must establish that it is the only possibility, not one of many that 'can be used.'

Because both Tavallaei and Olarig fail to teach or suggest any of the recited scaleable node controller, scalability port switch, or an address for the scaleable node controller, claims 1, 9 and 18 are not anticipated by either Tavallaei or Olarig. The dependent claims are likewise patentable.

With respect to claims 11 and 20, the office action identifies col. 7 lines 41-44 of Tavallaei for the recited comparing a priority of the interrupt request with a priority of the processor. However, the cited portion makes no reference whatsoever to a priority of the processor. Accordingly, claims 11 and 20 are separately patentable over Tavallaei.

With respect to claims 11 and 20, the office action identifies col. 10, lines 8-10 of Olarig for the recited comparing a priority of the interrupt request with a priority of the processor. In the Examiner's response to arguments, in numbered paragraph 61, the Examiner further identifies col. 3, lines 4-7 for this recitation. Col. 3, lines 4-7 discusses only comparing the priority of the interrupt with priorities of other tasks. Col. 10, lines 8-10 (which has no connection with the other cited portion of col. 3, lines 4-7) discusses only comparing a processor task priority level with other processors to select the least busy processor. However, neither cited portion makes any reference whatsoever to comparing a priority of the interrupt request with a priority of the processor. Accordingly, claims 11 and 20 are separately patentable over Olarig.

In numbered paragraph 59, the Examiner relies on page 8, lines 16-17 of the present specification to improperly read limitations from the specification into the claims. The Review Panel is respectfully directed to page 5, lines 25-27 of the present specification.

Claims 4 and 5 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Tavallaei in view of U.S. Patent No. 6,119,191 (Neal). The Examiner commits the following clear errors in making this rejection.

First, no one skilled in the art would be motivated to replace the ASIC 28 of Tavallaei with the hubs described in Neal. Second, the Examiner performs another clearly erroneous and overly broad claim construction. The Review Panel should ask itself, would one of

ordinary skill in the art as of December 29, 2000, without any knowledge of applicants' own invention, consider the ASIC 28 described by Neal to be an I/O hub? Applicants submit that the answer is clearly no, and that the claim construction set forth in the office action is a clearly erroneous attempt to stretch the reference beyond any reasonable reading in order to anticipate the claim.

Claims 6 and 7 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Tavallaei, in view of Neal, and further in view of Intel's Multiprocessor Specification, dated May 1997 (MP). The Examiner commits the following clear error in making this rejection.

As noted in applicants' response filed August 18, 2006, the Examiner has not even attempted to read the references on several recitations of claim 6 and claim 7. Accordingly, the Examiner fails to establish a prima facie case of obviousness and because Olarig does not teach or suggest two pair of scaleable node controllers with each pair connected to two different scalability port switches.

Claims 13 and 22 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Tavallaei in view of U.S. Patent No. 6,189,065 (Arndt). Claims 13 and 22 are also rejected under 35 U.S.C. § 103(a) as being unpatentable over Olarig in view of Arndt. The Examiner commits the following clear errors in making this rejection.

For the Review Panel's convenience, the claim language, the Examiner's stated rejection, and the cited portion of Arndt are reproduced below:

| | |
|---|---|
| Claims 13 and 22 | ... wherein said scalable node controller redirects the interrupt request through the scalability port switch to a different processor. |
| Examiner's rejection | ... Arndt discloses redirecting an interrupt to a different processor. Therefore it would have been obvious to combine the teachings of Arndt and [the primary reference] to redirect an interrupt to different processor since ... |
| Claim 8 Of Arndt | ... an offload selector for offloading said interrupt message to a second processor if said first processor is busy servicing another interrupt signal ... |

The claim language does not recite 'redirect an interrupt to a different processor'. The claim language recites that the scaleable node controller redirects the interrupt request through the scalability port switch to a different processor. The office action completely fails to address several of the claim recitations, and accordingly fails to establish a prima facie case of

obviousness. The Examiner's response to arguments, in numbered paragraph 61, fails to clarify or explain the Examiner's position or answer applicants' previous traversal. In any event, the cited portion of Arndt is silent in regard to these claim recitations.

Because the Arndt fails to make up for the respective deficiencies in Tavallaei and Olarig, and because there is no motivation to combine the references as suggested by the office action, and because the Examiner fails to establish a prima facie case of obviousness, and because the cited portion of Arndt fails to describe that a scalable node controller redirects the interrupt request through a scalability port switch to a different processor, claims 13 and 22 are separately patentable over the cited combination of references.

In view of the foregoing, favorable reconsideration and allowance of the application is respectfully requested. Early notification of the same is earnestly solicited. If there are any questions regarding the present application, the Review Panel is invited to contact the undersigned attorney at the telephone number listed below.

Respectfully submitted,

September 18, 2006
Date

/Paul E. Steiner/
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